What is claimed is:

1. An apparatus comprising:

a processor;

an expander memory bridge location;

a memory coupled to the expander memory bridge location; and

a controller including intercept logic to intercept and block communication from the processor to the expander memory bridge location and to emulate an expander memory bridge.

2. The apparatus of claim 1, wherein the controller includes a disable intercept logic bit.

3. The apparatus of claim 2, wherein the memory includes a mirror configuration.

4. The apparatus of claim 2, wherein the memory includes a redundant array of independent memories.

5. The apparatus of claim 3, wherein the processor includes a complex instruction set processor.

6. The apparatus of claim 1, wherein the bus controller includes an expander memory bridge plugged-in bit.

7. The apparatus of claim 6, wherein the memory includes a double data rate memory.

8. The apparatus of claim 1, further comprising an operating system to operate in cooperation with the processor, the operating system free of support for hot-pluggable components.

9. A method comprising:

intercepting and blocking a status request to a device, regardless of whether the device is installed; and

responding to the status request.

10. The method of claim 9, wherein intercepting and blocking the status request to the device, regardless of whether the device is installed, includes intercepting and blocking the status request during a configuration access to the device.

11. The method of claim 10, wherein responding to the status request includes emulating a response the device returns when the status request is not blocked.

12. The method of claim 11, wherein emulating a response the device returns when the status request is not blocked includes emulating the response of a memory bridge.

13. The method of claim 9, wherein responding to the status request includes responding that the device is available when the device is not installed.

14. The method of claim 13, wherein responding to the status request includes responding to the status request in a time period substantially equivalent to the time period in which a non-intercepted status request is responded to.

15. The method of claim 14, wherein intercepting and blocking the status request to the device, regardless of whether the device is installed, includes intercepting the status request directed to configuration space.

16. The method of claim 9, further comprising, removing the device, if the device is installed.

17. The method of claim 16, wherein removing the device, if the device is installed, includes removing a memory device.

18. The method of claim 9, further comprising, adding the device, if the device is not installed.

19. The method of claim 18, wherein adding the device if the device is not installed, includes adding a double data rate memory device.

20. A method comprising:

intercepting and blocking communications from a processor to an expander memory bridge; and

setting a disable intercept bit to stop interception and blocking of communications from the processor to the expander memory bridge.

21. The method of claim 20, further comprising configuring the expander memory bridge.

22. The method of claim 21, further comprising resetting the disable intercept bit.

23. A method comprising:

receiving control from an operating system after an interrupt;

polling a device plugged-in bit;

directing removal of a device, if the device plugged-in bit is active;

polling the device plugged-in bit; and

returning control to the operating system when the device plugged-in bit is inactive.

24. The method of claim 23, wherein directing removal of the device, if the device plugged-in bit is active, includes directing removal of an expander memory module.

25. The method of claim 24, wherein polling the device plugged-in bit includes polling a controller that provides the device plugged-in bit.

26. A system comprising:

a processor;

an expander memory bridge location;

a memory coupled to the expander memory bridge location;

a controller including intercept logic to intercept and block communication from the processor to the expander memory bridge location and to emulate an expander memory bridge;

a display coupled to the processor; and

a storage device coupled to the processor.

27. The system of claim 26, wherein the display comprises a plasma display.

28. The system of claim 26, wherein the storage device comprises a magnetic storage device.